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How to download Secrets can kill ebook on free download for iphone? The present invention relates to a method for manufacturing a semiconductor device. More particularly, it relates to a method for forming source/drain regions of a semiconductor device on a semiconductor substrate having a structure where source/drain regions are arranged on a p-type well region and an n-type well region at the same time. When a field effect transistor is manufactured, it is required to form source/drain regions of the transistor which have a desired shape and size. In order to meet this requirement, it is required to arrange the source/drain regions at the desired positions on the substrate. A conventional semiconductor device in which a field effect transistor is formed will be described below with reference to the cross-sectional views of FIGS. 5(a) to 5(c). As shown in FIG. 5(a), a p-type well region 2 is formed on the surface of a silicon substrate 1 having an n-type well region 3 formed thereon. On the surface of the p-type well region 2, a semiconductor device is formed. A field effect transistor 4 is formed on the surface of the semiconductor device. An isolation oxide film 5 is formed between the transistors 4 and 5, so as to electrically separate the transistors. On the surface of the semiconductor device, an aluminum interconnection layer 6 is formed which is connected to the field effect transistor 4. As shown in FIG. 5(b), the field effect transistor 4 includes a gate electrode 7 formed on the p-type well region 2, a pair of n-type source/drain regions 8a and 8b which are formed on the surface of the p-type well region 2 on both sides of the gate electrode 7, and a region forming an extension region 8c which is formed on the surface of the p-type well region 2 between the n-type source/drain regions 8a and 8b. The region forming the extension region 8c is obtained by forming ntype regions 9 in the surface of the p-type well region 2 between the source/drain regions 8a and 8b. As shown in FIG. 5(c), on the surface of the n-type well region 3, a field oxide film 10 is formed to isolate the transistor 5 from other transistors. The field effect transistor 5 is formed in the n-type well region 3. A

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